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jc952 U.S. PTO

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A

IN THE U.S. PATENT AND TRADEMARK OFFICE

Attorney Docket No.: 121251-1016

Box: Patent Application  
Commissioner for Patents  
Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor: John L. Pierce of Dallas, Texas

For: System. Method and Apparatus For Constructing A Semiconductor Wafer-Interposer Using B-Stage Laminates

Enclosed are: 3 sheet(s) of informal drawings;  
13 pages of Specification;  
9 pages of Claims; and  
1 page of Abstract.

Enclosed please also find an executed Declaration/Power of Attorney.

This Patent has been assigned to Micro-ASI, Inc., 12655 North Central Expressway, Suite 1000, Dallas, Texas 75243 which qualifies for Small Entity Status.

"Express Mail" mailing label number EL417462232US  
Date of Deposit: December 15, 2000. I certify that the accompanying Application is being deposited with the United States Postal Service "Express Mail Post Office to addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application, Commissioner for Patents, Washington, DC 20231.

*Heather R. Huse*  
Heather R. Huse

JC760 U.S. PTO  
09/738193  
12/15/00

FEE CALCULATION					FEE
	NUMBER		NUMBER EXTRA	RATE	BASIC FEE \$355.00
Total Claims	31	- 20 =	11	x \$9=	\$ 99.00
Independent Claims	4	- 3 =	1	x \$40 =	\$ 40.00
TOTAL FEES					\$ 552.00

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 07-0153.

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All correspondence related to this application may be addressed to the undersigned at Gardere Wynne Sewell, LLP,  
3000 Thanksgiving Tower, 1601 Elm Street Suite 3000, Dallas, Texas 75201-4767.

December 15, 2000

Date



Daniel J. Chalker  
Attorney for Applicant(s)  
Reg. No. 40,552

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**GARDERE**

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December 15, 2000

BOX NEW APP/FEE  
Assistant Commissioner for Patents  
Washington, D.C. 20231

**VIA EXPRESS MAIL NO. EL417462232US**

Re: Patent Application for "System, Method And Apparatus For Constructing A Semiconductor Wafer-Interposer Using B-Stage Laminates"  
Our File No.: 121251-1016

Dear Sir:

Enclosed for filing for the above referenced patent application, please find the following:

- (1) Patent Application;
- (2) Transmittal Form;
- (3) Check for \$552.00;
- (4) Declaration/Power of Attorney; and
- (5) Return Postcard.

Please file the above documents and return the file-stamped postcard to our offices.

Thank you for your assistance. Should you have any questions, please call me.

Respectfully submitted,

GARDERE WYNNE SEWELL, LLP.



Daniel J. Chalker  
Registration No. 40,552

DJC/hrh

Enclosures

cc: Sanford E. Warren, Jr.

DALLAS 954754v1

PATENT APPLICATION SERIAL NO. \_\_\_\_\_

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE  
FEE RECORD SHEET

12/20/2000 EEKUBAY1 00000116 09738193

01 FC:201	355.00	OP
02 FC:202	40.00	OP
03 FC:203	99.00	OP

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